IN THE CLAIMS

Amend Claims 1, 5, 6, 8, 12, 16 - 19, 23, 31, 38, 39, and 41, cancel Claims 3 and 43 - 80 without prejudice, and add new Claims 81 - 105 so that the claims are as follows:

1. (Currently amended) A structure comprising:

an n-channel surface-channel insulated-gate field-effect transistor ("SCIGFET") comprising a pair of laterally separated n-type source/drain zones situated in a semiconductor body along a major surface thereof, a p-type channel zone situated between the n-channel SCIGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the n-channel SCIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel SCIGFET from its source/drain and channel zones; and

a normally off n-channel channel-junction insulated-gate field-effect transistor ("CJIGFET") comprising a pair of laterally separated n-type source/drain zones situated in the semiconductor body along its major surface, an n-type channel zone extending between the n-channel CJIGFET's source/drain zones in the semiconductor body along its major surface and more lightly doped than the n-channel CJIGFET's source/drain zones, a gate electrode situated over the channel zone of the n-channel CJIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel CJIGFET from its source/drain and channel zones, the gate dielectric layer of the n-channel CJIGFET being materially thicker than the gate dielectric layer of the n-channel SCIGFET.

2. (Original) A structure as in Claim 1 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrode of the n-channel CJIGFET comprises p-type semiconductor material.

3. (Canceled)

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4. (Original) A structure as in Claim 1 wherein the n-channel CJIGFET is of greater channel length than the n-channel SCIGFET.

5. (Currently amended) A structure as in Claim 1 wherein the n-channel CJIGFET is of dimensions and dopant concentrations so as to conduct ~~conducts~~ current through a field-induced surface channel that extends across the channel zone of the n-channel CJIGFET substantially up to its gate dielectric layer.

6. (Currently amended) A structure as in Claim 1 wherein the n-channel CJIGFET is of dimensions and dopant concentrations so as to conduct ~~conducts~~ current through a metallurgical subsurface channel that extends across the channel zone of the n-channel CJIGFET below, and spaced apart from, its gate dielectric layer.

7. (Original) A structure as in Claim 1 wherein the channel and source/drain zones of the n-channel CJIGFET contain arsenic as n-type dopant.

8. (Currently amended) A structure as in Claim 1 further ~~1further~~ including a p-channel SCIGFET comprising a pair of laterally separated p-type source/drain zones situated in the semiconductor body along its major surface, an n-type channel zone extending between the p-channel SCIGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the p-channel SCIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the p-channel SCIGFET from its source/drain and channel zones.

9. (Original) A structure as in Claim 8 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET and the n-channel CJIGFET comprise p-type semiconductor material.

10. (Original) A structure as in Claim 9 wherein the semiconductor material of the gate electrodes comprises non-monocrystalline semiconductor material.

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11. (Original) A structure as in Claim 10 wherein the non-monocrystalline semiconductor material comprises polycrystalline semiconductor material.

12. (Currently amended) A structure as in Claim 8 wherein the gate dielectric layer of the n-channel CJIGFET is also materially thicker than the gate dielectric layer of the p-channel SCIGFET. ~~layers of the two SCIGFETs.~~

13. (Original) A structure as in Claim 12 wherein the gate dielectric layers of the two SCIGFETs are of approximately equal thickness.

14. (Original) A structure as in Claim 12 wherein the n-channel CJIGFET is of greater channel length than each SCIGFET.

15. (Original) A structure as in Claim 12 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET and the n-channel CJIGFET comprise p-type semiconductor material.

16. (Currently amended) A structure as in Claim 8 wherein the n-channel CJIGFET is of dimensions and dopant concentrations so as to conduct ~~conducts~~ current through a field-induced surface channel that extends across the channel zone of the n-channel CJIGFET substantially up to its gate dielectric layer.

17. (Currently amended) A structure as in Claim 16 wherein the gate dielectric layer of the n-channel CJIGFET is also materially thicker than the gate dielectric layer of the p-channel SCIGFET. ~~layers of the two SCIGFETs.~~

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18. (Currently amended) A structure as in Claim 8 wherein the n-channel CJIGFET is of dimensions and dopant concentrations so as to conduct ~~conducts~~ current through a metallurgical subsurface channel that extends across the channel zone of the n-channel CJIGFET below, and spaced apart from, its gate dielectric layer.

19. (Currently amended) A structure as in Claim 18 wherein the gate dielectric layer of the n-channel CJIGFET is also materially thicker than the gate dielectric layer of the p-channel SCIGFET. ~~layers of the two SCIGFETs.~~

20. (Original) A structure as in Claim 8 wherein the channel and source/drain zones of the n-channel CJIGFET contain arsenic as n-type dopant.

21. (Original) A structure as in Claim 8 wherein the channel zone of each SCIGFET is part of body material having a net dopant concentration which reaches a primary local subsurface maximum below a channel surface depletion region that extends along the semiconductor body's major surface into that channel zone but no more than 0.4 μm below the semiconductor body's major surface.

22. (Original) A structure as in Claim 21 wherein the net dopant concentration of the body material for each SCIGFET reaches a pair of additional vertically separated local subsurface maxima deeper below the semiconductor body's major surface than the primary local subsurface maximum in the net dopant concentration for that body material.

23. (Currently amended) A structure as in Claim 8 wherein the source/drain and channel zones of the n-channel CJIGFET form a composite pn junction with body material having a net dopant concentration which reaches a primary local subsurface maximum below the channel zone of the n-channel CJIGFET but no more than 0.6 μm below the semiconductor body's major surface.

24. (Original) A structure as in Claim 23 wherein the net dopant concentration of the body material for the n-channel CJIGFET reaches a pair of additional vertically separated subsurface maxima deeper below the semiconductor body's major surface than the primary local subsurface maximum in the net dopant concentration for that body material.

25. (Original) A structure as in Claim 8 wherein the channel zone of each SCIGFET has a net dopant concentration which reaches a local subsurface minimum along the semiconductor body's major surface at a location between that SCIGFET's source/drain zones.

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26. (Original) A structure as in Claim 25 wherein the channel zone of each SCIGFET is part of body material having a net dopant concentration which reaches a primary local subsurface maximum below a channel surface depletion region that extends along the semiconductor body's major surface into that channel zone but no more than 0.4 μm below the semiconductor body's major surface.

27. (Original) A structure as in Claim 8 wherein the three gate dielectric layers comprise semiconductor material and oxygen.

28. (Original) A structure as in Claim 27 wherein the gate dielectric layers of the two SCIGFETs further include nitrogen.

29. (Original) A structure as in Claim 27 wherein the semiconductor body and the semiconductor material in the three gate dielectric layers both comprise silicon.

30. (Original) A structure as in Claim 8 where each source/drain zone comprises a main source/drain portion and a more lightly doped source/drain extension laterally continuous with the main source/drain portion, the source/drain extensions of the two source/drain zones of each transistor terminating its channel zone along the semiconductor body's major surface.

31. (Currently amended) A structure as in Claim 8 further including a normally off p-channel further insulated-gate field-effect transistor ("IGFET") comprising a pair of laterally separated p-type source/drain zones situated in the semiconductor body along its major surface, a channel zone extending between the p-channel further IGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the p-channel further IGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the p-channel further IGFET from its source/drain and channel zones, the gate dielectric layers of the n-channel CJIGFET and the p-channel further IGFET both being <u>materially</u> thicker than the gate dielectric layers of the two SCIGFETs.

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32. (Original) A structure as in Claim 31 wherein:

the gate dielectric layers of the two SCIGFETs are of approximately equal thickness; and

the gate dielectric layers of the n-channel CJIGFET and the p-channel further IGFET are of approximately equal thickness.

33. (Original) A structure as in Claim 31 wherein the n-channel CJIGFET and the p-channel further IGFET are each of greater channel length than each SCIGFET.

34. (Original) A structure as in Claim 31 wherein the channel zone of the p-channel further IGFET is n-type such that the p-channel further IGFET is an SCIGFET.

35. (Original) A structure as in Claim 34 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET, the n-channel CJIGFET, and the p-channel further IGFET comprise p-type semiconductor material.

36. (Original) A structure as in Claim 31 wherein the channel zone of the p-channel further IGFET is p-type and is more lightly doped than its source/drain zones such that the p-channel further IGFET is a CJIGFET.

37. (Original) A structure as in Claim 36 wherein:

the gate electrodes of the n-channel SCIGFET and the p-channel further IGFET comprise n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET and the n-channel CJIGFET comprise p-type semiconductor material.

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38. (Currently amended) A structure as in Claim 31 wherein the n-channel CJIGFET is of dimensions and dopant concentrations so as to conduct ~~conducts~~ current through a field-induced surface channel that extends across the channel zone of the n-channel CJIGFET substantially up to its gate dielectric layer.

39. (Currently amended) A structure as in Claim 31 wherein the n-channel CJIGFET is of dimensions and dopant concentrations so as to conduct ~~conducts~~ current through a metallurgical subsurface channel that extends across the channel zone of the n-channel CJIGFET below, and spaced apart from, its gate dielectric layer.

40. (Original) A structure as in Claim 31 wherein the channel zone of each SCIGFET is part of body material having a net dopant concentration which reaches a primary local subsurface maximum below a channel surface depletion region that extends along the semiconductor body's major surface into that channel zone but no more than 0.4 µm below the semiconductor body's major surface.

41. (Currently amended) A structure as in Claim 31 wherein the source/drain and channel zones of the n-channel CJIGFET form a composite pn junction with body material having a net dopant concentration which reaches a primary local subsurface maximum below the channel zone of the n-channel CJIGFET but no more than 0.6 µm below the semiconductor body's major surface.

42. (Original) A structure as in Claim 31 wherein the channel zone of each SCIGFET is part of body material having a net dopant concentration which reaches a primary local subsurface maximum below a channel surface depletion region that extends along the semiconductor body's major surface into that channel zone but no more than 0.4 µm below the semiconductor body's major surface.

43 - 80. (Canceled)

81. (New) A structure as in Claim 1 the gate dielectric layer of the n-channel CJIGFET is at least twice as thick as the gate dielectric layer of the n-channel SCIGFET.

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82. (New) A structure as in Claim 1 further including circuitry for providing voltages to the n-channel CJIGFET and the n-channel SCIGFET and for operating the n-channel CJIGFET across a materially greater voltage range than the n-channel SCIGFET.

83. (New) A structure as in Claim 82 wherein the voltage-providing/operating circuitry comprises:

analog circuitry for providing voltages to the n-channel CJIGFET; and

digital circuitry for providing voltages to the n-channel SCIGFET.

84. (New) A structure as in Claim 12 the gate dielectric layer of the n-channel CJIGFET is at least twice as thick as the gate dielectric layer of each of the two SCIGFETs.

85. (New) A structure as in Claim 12 further including circuitry for providing voltages to the n-channel CJIGFET and the two SCIGFETs and for operating the n-channel CJIGFET across a materially greater voltage range than the two SCIGFETs.

86. (New) A structure as in Claim 85 wherein the voltage-providing/operating circuitry comprises:

analog circuitry for providing voltages to the n-channel CJIGFET; and

digital circuitry for providing voltages to the two SCIGFETs.

87. (New) A structure as in Claim 17 the gate dielectric layer of the n-channel CJIGFET is at least twice as thick as the gate dielectric layer of each of the two SCIGFETs.

88. (New) A structure as in Claim 17 further including circuitry for providing voltages to the n-channel CJIGFET and the two SCIGFETs and for operating the n-channel CJIGFET across a materially greater voltage range than the two SCIGFETs.

89. (New) A structure as in Claim 19 the gate dielectric layer of the n-channel CJIGFET is at least twice as thick as the gate dielectric layer of each of the two SCIGFETs.

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90. (New) A structure as in Claim 19 further including circuitry for providing voltages to the n-channel CJIGFET and the two SCIGFETs and for operating the n-channel CJIGFET across a materially greater voltage range than the two SCIGFETs.

91. (New) A structure as in Claim 31 the gate dielectric layer of each of the n-channel CJIGFET and the p-channel further IGFET is at least twice as thick as the gate dielectric layer of each of the two SCIGFETs.

92. (New) A structure as in Claim 31 further including circuitry for providing voltages to the n-channel CJIGFET, the two SCIGFETs, and the p-channel further IGFET and for operating the n-channel CJIGFET and the p-channel further IGFET across a materially greater voltage range than the two SCIGFETs.

93. (New) A structure as in Claim 92 wherein the voltage-providing/operating circuitry comprises:

analog circuitry for providing voltages to the n-channel CJIGFET and the p-channel further IGFET; and

digital circuitry for providing voltages to the two SCIGFETs.

94. (New) A structure comprising:

an n-channel surface-channel insulated-gate field-effect transistor ("SCIGFET") comprising a pair of laterally separated n-type source/drain zones situated in a semiconductor body along a major surface thereof, a p-type channel zone situated between the n-channel SCIGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the n-channel SCIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel SCIGFET from its source/drain and channel zones; and

a normally off n-channel channel-junction insulated-gate field-effect transistor ("CJIGFET") comprising a pair of laterally separated n-type source/drain zones situated in the semiconductor body along its major surface, an n-type channel zone extending between the n-channel CJIGFET's source/drain zones in the semiconductor body along its major surface and more lightly doped than the n-channel CJIGFET's source/drain zones, a gate electrode situated over the channel zone of the n-channel CJIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel CJIGFET from its source/drain and channel zones, the n-channel CJIGFET being of dimensions and dopant concentrations so as to conduct current through a field-induced surface channel that extends across the channel zone of the n-channel CJIGFET substantially up to its gate dielectric layer.

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95. (New) A structure as in Claim 94 wherein the n-channel CJIGFET is of greater channel length than the n-channel SCIGFET.

96. (New) A structure as in Claim 94 further including circuitry for providing voltages to the n-channel CJIGFET and the n-channel SCIGFET and for operating the n-channel CJIGFET across a materially greater voltage range than the n-channel SCIGFET.

97. (New) A structure as in Claim 96 wherein the voltage-providing/operating circuitry comprises:

analog circuitry for providing voltages to the n-channel CJIGFET; and
digital circuitry for providing voltages to the n-channel SCIGFET.

98. (New) A structure as in Claim 94 further including a p-channel SCIGFET comprising a pair of laterally separated p-type source/drain zones situated in the semiconductor body along its major surface, an n-type channel zone extending between the p-channel SCIGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the p-channel SCIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the p-channel SCIGFET from its source/drain and channel zones.

99. (New) A structure as in Claim 98 wherein the n-channel CJIGFET is of greater channel length than each SCIGFET.

100. (New) A structure as in Claim 98 further including circuitry for providing voltages to the n-channel CJIGFET and the two SCIGFETs and for operating the n-channel CJIGFET across a materially greater voltage range than the two SCIGFETs.

101. (New) A structure as in Claim 100 wherein the voltage-providing/operating circuitry comprises:

analog circuitry for providing voltages to the n-channel CJIGFET; and
digital circuitry for providing voltages to the two SCIGFETs.

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102. (New) A structure as in Claim 98 further including a normally off p-channel further insulated-gate field-effect transistor ("IGFET") comprising a pair of laterally separated p-type source/drain zones situated in the semiconductor body along its major surface, a channel zone extending between the p-channel further IGFET's source/drain zones in the

semiconductor body along its major surface, a gate electrode situated over the channel zone of the p-channel further IGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the p-channel further IGFET from its source/drain and channel zones.

103. (New) A structure as in Claim 102 wherein the n-channel CJIGFET and the p-channel further IGFET are each of greater channel length than each SCIGFET.

104. (New) A structure as in Claim 102 further including circuitry for providing voltages to the n-channel CJIGFET, the two SCIGFETs, and the p-channel further IGFET and for operating the n-channel CJIGFET and the p-channel further IGFET across a materially greater voltage range than the two SCIGFETs.

105. (New) A structure as in Claim 104 wherein the voltage-providing/operating circuitry comprises:

analog circuitry for providing voltages to the n-channel CJIGFET and the p-channel further IGFET; and

digital circuitry for providing voltages to the two SCIGFETs.

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